ROC920030018 PATENTS

**Amendments to the Claims**

**Please amend Claims 1-4, 6, 13-16, 18-28 and cancel Claim 17 without prejudice such that the pending claims will read as follows:**

1. (Currently Amended) A method for maintaining control structure coherency comprising:

writing a pointer to a control structure in a hardware update list while one or more portions of the control structure are accessed by ~~hardware~~ a logic device during a hardware update operation; and

delaying ~~a software access to~~ instructions executed by a processor from accessing the one or more portions of the control structure during a software update operation while the pointer to the control structure is on the hardware update list.

2. (Currently Amended) The method of claim 1 further comprising removing the pointer to the control structure from the hardware update list after the one or more ~~of the~~ portions of the control structure accessed by the ~~hardware~~ logic device during the hardware update operation are no longer accessed by the ~~hardware~~ logic device.

3. (Currently Amended) The method of claim 1 wherein writing the pointer to the control structure in the hardware update list while one or more portions of the control structure are accessed by ~~hardware~~ the logic device includes writing the pointer to the control structure in the hardware update list while all portions of the control structure are



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accessed by the ~~hardware~~ logic device during the hardware update operation.

4. (Currently Amended) The method of claim 1 wherein the software update operation includes updating a field of the control structure using instructions executed by the processor.

5. (Original) The method of claim 1 wherein the pointer represents at least a portion of an address of the control structure.

6. (Currently Amended) The method of claim 1 wherein the hardware update list is stored in ~~hardware~~ a logic device.

7. (Original) The method of claim 6 wherein the hardware update list is stored in at least one of memory and registers.

8. (Original) The method of claim 1 wherein the hardware update list includes a plurality of entries.

9. (Original) The method of claim 1 wherein the control structure includes a control block.

10. (Original) The method of claim 9 wherein a control block includes a plurality of bytes of data.



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11. (Original) The method of claim 9 wherein the control block includes information based on a cell or frame received by a network processor.

12. (Original) The method of claim 9 wherein the one or more portions of the control structure include one or more bytes of the control block.

13. (Currently Amended) The method of claim 1 wherein writing the pointer to the control structure in the hardware update list while one or more portions of the control structure are accessed by the ~~hardware~~ logic device during the hardware update operation includes writing the pointer to the control structure in the hardware update list while one or more pointers of the control structure are read from a memory, modified, and written back to the memory by the ~~hardware~~ logic device during the hardware operation.

14. (Currently Amended) The method of claim 1 wherein delaying the ~~software access~~ instructions executed by the processor from accessing the one or more portions of the control structure includes monitoring a bus for at least one of a control signal and an address.

15. (Currently Amended) The method of claim 14 wherein delaying the ~~software access~~ instructions executed by the processor from accessing the one or more portions of the control structure includes rejecting ~~software access to~~ the instructions executed by the processor at the bus while the pointer to the control structure is on the hardware update list.



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16. (Currently Amended) The method of claim 14 wherein delaying the ~~software access~~ instructions executed by the processor from accessing the one or more portions of the control structure includes:

granting a request for the ~~software access~~ instructions executed by the processor to access the one or more portions of the control structure; and

delaying the ~~software access~~ instructions executed by the processor while the pointer to the control structure is on the hardware update list.

17. (Canceled).

18. (Currently Amended) The method of claim 1 wherein delaying the ~~software access to one or more portions of the control structure~~ instructions executed by the processor from accessing the one or more portions of the control structure while the pointer to the control structure is on the hardware update list includes delaying at least one of a read, a modify and a write operation performed by software on the one or more portions of the control structure while the pointer to the control structure is on the hardware update list.

19. (Currently Amended) An apparatus comprising:

a hardware update logic device adapted to couple to a memory controller of a network processor and adapted to interact with an at least one memory so as to:

write a pointer to a control structure stored in the at least one memory in a hardware update list while one



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or more portions of the control structure are accessed by the hardware update logic device during a hardware update operation; and

delay ~~a software access to one or more portions of the control structure~~ instructions executed by the processor from accessing the one or more portions of the control structure during a software update operation while the pointer to the control structure is on the hardware update list.

20. (Currently Amended) The apparatus of claim 19 wherein the hardware update logic device is further adapted to remove the pointer to the control structure from the hardware update list after the one or more ~~of the~~ portions of the control structure accessed by the hardware update logic device during the hardware update operation are no longer accessed by the hardware update logic device.

21. (Currently Amended) The apparatus of claim 19 wherein the hardware update logic device is adapted to detect the ~~software access~~ instructions executed by the processor by employing the memory controller to monitor at least one of a control signal and an address on a bus.

22. (Currently Amended) The apparatus of claim 20 wherein the hardware update logic device is adapted to delay the ~~software access~~ instructions executed by the processor from accessing the one or more portions of the control structure by employing the memory controller to reject ~~software access to~~ instructions executed by the processor at



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the bus while the pointer to the control structure is on the hardware update list.

23. (Currently Amended) The apparatus of claim 20 wherein the hardware update logic device is adapted to delay the ~~software access~~ instructions executed by the processor from accessing the one or more portions of the control structure by employing the memory controller to:

grant a request for the ~~software access~~ instructions executed by the processor for accessing the one or more portions of the control structure; and

delay the ~~software access~~ instructions executed by the processor while the pointer to the control structure is on the hardware update list.

24. (Currently Amended) A network processor system comprising:

at least one memory adapted to store a plurality of control structures;

a network processor comprising:

a memory controller coupled to the at least one memory;

a hardware update logic device coupled to the memory controller and adapted to interact with the at least one memory so as to:

write a pointer to a control structure in a hardware update list while one or more portions of the control structure are accessed by the hardware update logic device during a hardware update operation; and

delay ~~a software access to~~ instructions executed by a processor from accessing the one or



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more portions of the control structure during a software update operation while the pointer to the control structure is on the hardware update list.

25. (Currently Amended) The network processor system of claim 24 wherein the hardware update logic device is further adapted to remove the pointer to the control structure from the hardware update list after the one or more ~~of the~~ portions of the control structure accessed by the hardware update logic device during the hardware update operation are no longer accessed by the hardware.

26. (Currently Amended) The network processor system of claim 24 wherein the hardware update logic is adapted to detect the ~~software access to~~ instructions executed by a processor by employing the memory controller to monitor at least one of a control signal and an address on a bus.

27. (Currently Amended) The network processor system of claim 24 wherein the memory controller includes the hardware update logic device.

28. (Currently Amended) The network processor system of claim 27 wherein the hardware update logic device includes on-chip memory.

29. (Original) The network processor system of claim 24 further comprising a plurality of processors coupled to the memory controller using an internal bus.



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30. (Original) The network processor system of claim 24 wherein the at least one memory includes a DRAM.



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